



8051 Assembly Language Programming

Chapter Objectives

- List the registers of the 8051 microcontroller
- Manipulate data using the registers and MOV instructions
- Code Simple 8051 Assembly Language Instructions
- Assemble and run an 8051 program



8051 Flag Bits and the PSW Registers

Program Status Word Registers

- The 8051 μ C has a flag register to indicate arithmetic conditions such as the carry bit.
- The flag register in the 8051 is called the ***program status word*** (PSW).
- The program status word (PSW) register is an 8bit register. It is also referred to as the ***flag register***.
- The PSW register is 8 bits wide but only 6bits are used by the 8051.
- The 2 unused bits are ***user-definable flags***.

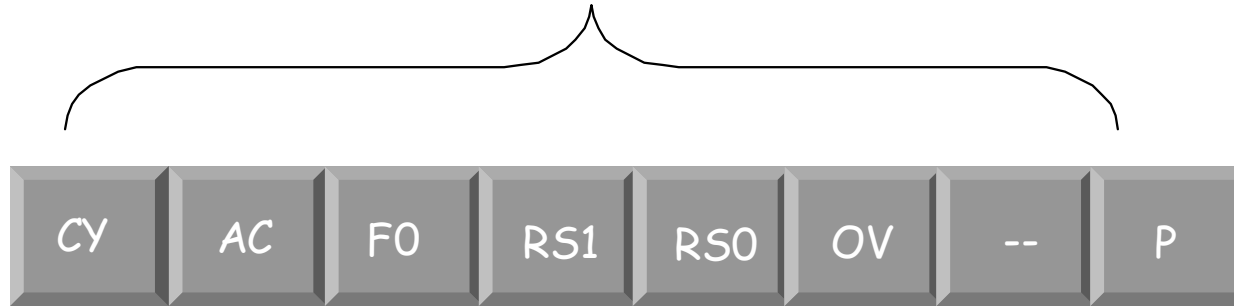


8051 Flag Bits and the PSW Registers

Program Status Word Registers...

- Four of the flags are called conditional flags, meaning that they indicate some conditions that result after an instruction is executed.
- The four flags are **CY** (Carry), **AC** (Auxiliary Carry), **P** (Parity), and **OV** (Overflow). See Figure 2-1.
- Bits PSW.3 and PSW.4 are designated as RS0 and RS1, respectively.
- They are used to change the bank registers.
- Bits PSW.1 and PSW.5 are general purpose status flags and can be used by the programmer for any purpose. (User Definable)

Figure 2-1:PSW Register Bits



CY	PSW.7	Carry flag
AC	PSW.6	Auxiliary carry flag
F0	PSW.5	Available to the user for general purpose
RS1	PSW.4	Register Bank selector bit 1
RS0	PSW.3	Register Bank selector bit 0
OV	PSW.2	Overflow flag
--	PSW.1	User-definable bit
P	PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of 1 bits in the accumulator.

RS1	RS0	Register Bank	Address
0	0	0	00H - 07H
0	1	1	08H - 0FH
1	0	2	10H - 17H
1	1	3	18H - 1FH



8051 Flag Bits and the PSW Registers

Program Status Word Registers

CY, the carry flag – This flag is set whenever there is a carry out from D7 bit.

- Affected after an 8bit addition or subtraction operation.
- Can be used to set “1” or “0” directly by an instruction such as “SETB C” and “CLR C” where “SETB C” stands for “***set bit carry***” and “CLR C” for “***clear carry***”.

AC, the auxiliary carry flag – If there is a carry from D3 to D4 during an ADD or SUB operation, this bit is set, otherwise, it’s cleared.

- This flag is used by instructions that perform BCD (Binary Coded Decimal) arithmetic



8051 Flag Bits and the PSW Registers

Program Status Word Registers

P, the parity flag

- The parity flag reflects the number of 1s in the A (accumulator) register only.
- If the A register contains an odd number of 1s, then $P=1$
- Therefore, $P=0$ if A has an even number of 1s.

OV, the overflow flag

- This flag is set whenever the result of a signed number operation is too large.
- Causes the high-order bit to overflow into the sign bit.



8051 Flag Bits and the PSW Registers

Program Status Word Registers...

OV, the overflow flag

- The carry flag is used to detect errors in unsigned arithmetic operations.
- The overflow flag is only used to detect errors in signed arithmetic operations.



8051 Flag Bits and the PSW Registers

ADD instruction and PSW registers

The following table illustrates the affect basic arithmetic operations have on the PSW registers

Instructions That Affect Flag Bits

Instruction	CY	OV	AC
ADD	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	0	X	
DIV	0	X	
DA	X		
RRC	X		
RLC	X		
SETB C	1		
CLR C	0		
CPL C	X		
ANL C, bit	X		
ANL C, /bit	X		
ORL C, bit	X		
MOV C, bit	X		
CJNE	X		

Note: X can be 0 or 1



8051 REGISTER BANKS AND STACK

RAM memory space allocation in the 8051

- The 8051 microcontroller has a total of 128 bytes of RAM.
- Some members notably the 8052 have 256 bytes of RAM.
- The 128 bytes of RAM, inside the 8051 are assigned addresses 00 to 7FH.
- These 128 bytes are divided into 3 different groups
 - a) A total of 32 bytes from locations 00 to 1F hex are set aside for register banks and the stack.
 - b) A total of 16 bytes from locations 20H to 2FH are set aside for bit addressable read/write memory.



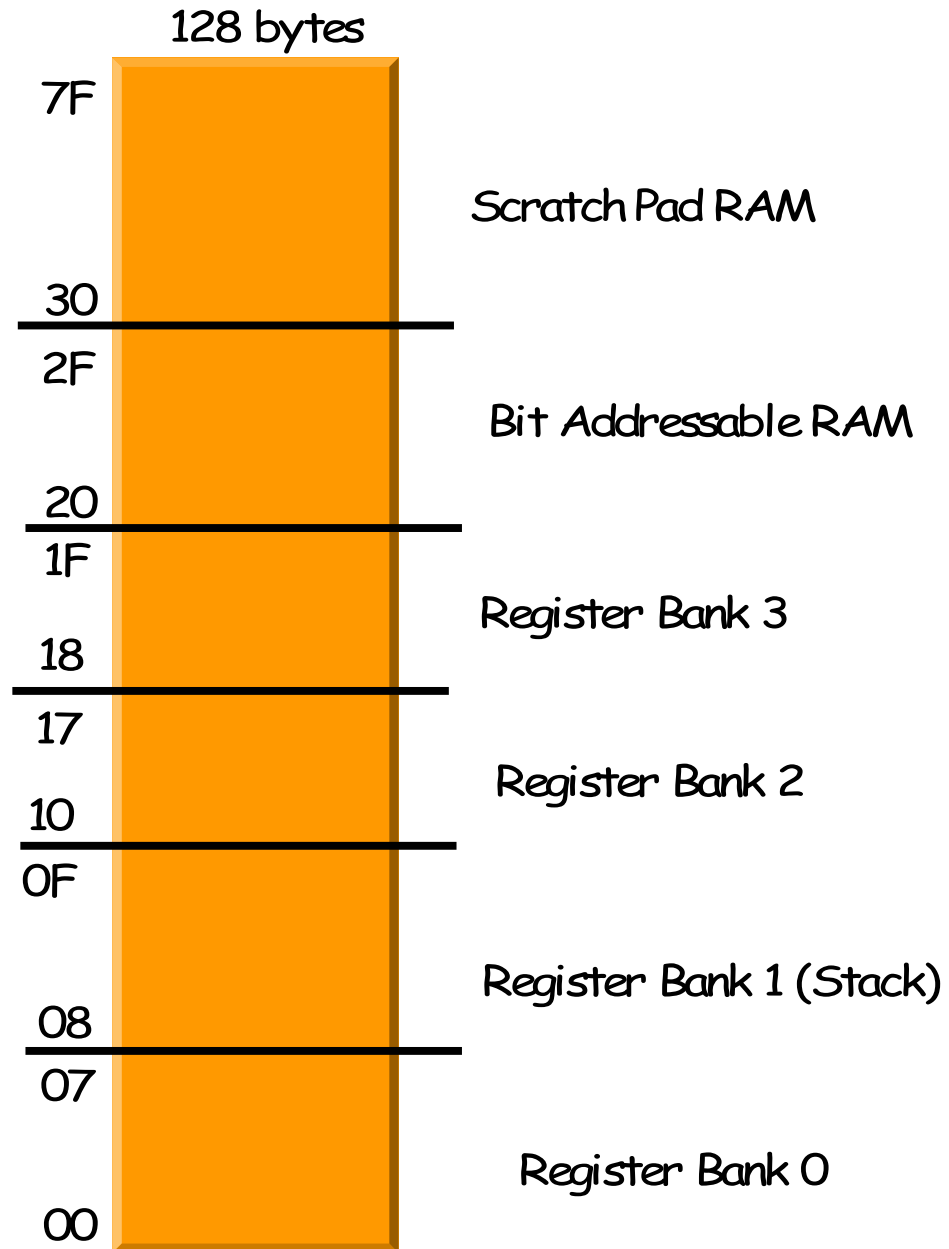
8051 REGISTER BANKS AND STACK

RAM memory space allocation in the 8051...

- c) A total of 80 bytes from locations 30H to 70H are used for read and write storage, or what is normally called a scratch pad.
 - i. These 80 locations of RAM are widely used for the purpose of storing data and parameters by 8051 programmers.
 - ii. They will be used to store data brought into the CPU via I/O ports.

See Figure 2-2 for RAM Allocation in the 8051.

Figure 2-2.
RAM Allocation in
the 8051





8051 REGISTER BANKS AND STACK

Register banks in the 8051

- A total of 32 bytes of RAM are set aside for the register and banks.
- These 32 bytes are divided into 4 banks of registers in which each bank has 8 registers, R0 - R7.
- RAM locations from 0 - 7 are set aside for bank 0 of R0 - R7 (where R0 is RAM location 0, R1 is RAM location 1, R2 is location 2, and so on).
- 7 belongs to R7 of bank 0.
- The second bank of registers R0 - R7 starts at RAM location 08 and goes to location 17H.



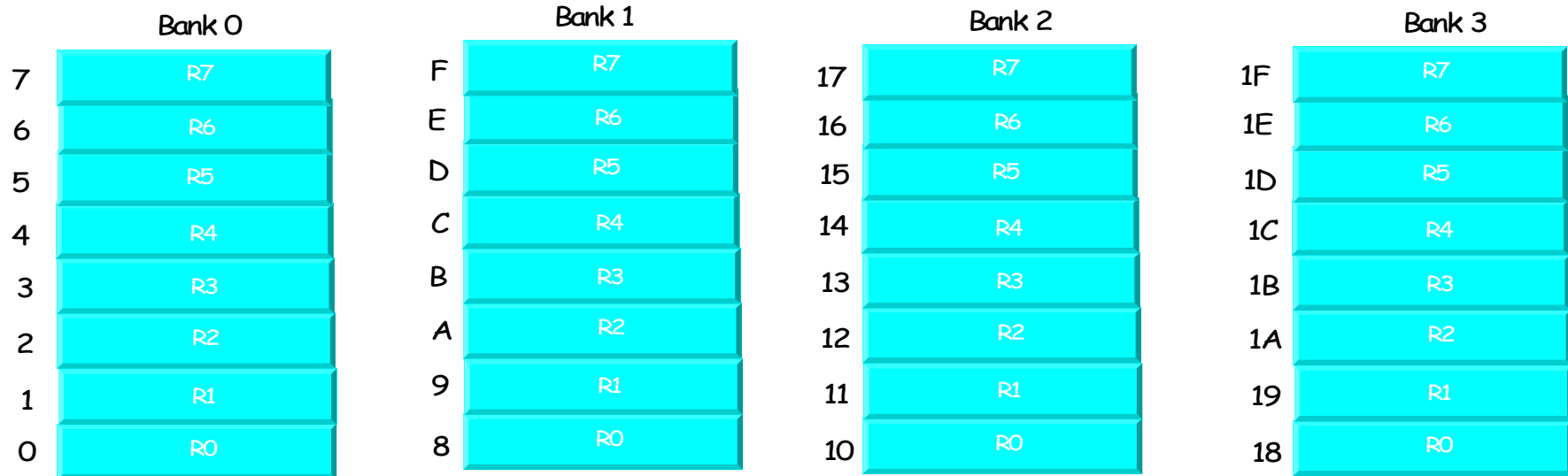
8051 REGISTER BANKS AND STACK

Register banks in the 8051...

- Finally, RAM locations 18H - 1FH are set aside for the 4th bank of R0 - R7.

Figure 2-3 illustrates the Register Banks and their RAM addresses.

Figure 2-3. 8051 Register Banks and their RAM Addresses





8051 REGISTER BANKS AND STACK

How to switch register banks

The following table illustrates the selection of Banks using the PSW(program status word) register (Bits D4 and D3 are used).

PSW Bits Bank Selection

	RS1 (PSW.4)	RS0 (PSW.3)
Bank 0	0	0
Bank 1	0	1
Bank 2	1	0
Bank 3	1	1



8051 REGISTER BANKS AND STACK

Stack in the 8051

- The stack is a section of RAM used by the CPU to store information temporarily.
- The information store could be data or an address
- The CPU needs this storage area since there only a limited number of registers.



8051 REGISTER BANKS AND STACK

How stacks are accessed in the 8051

- If the stack is a section of RAM, there must be registers inside the CPU to point to.
- The register used to access the stack is called the **SP** (Stack Pointer).
- The stack pointer in the 8051 is only 8 bits wide: it can take values of 00H to FFH.
- When the 8051 is powering up, the SP contains value 07.
- This means the RAM location 08 is the first location used for the stack by the 8051.
- The storing of a CPU register in the stack is called a **PUSH**.



8051 REGISTER BANKS AND STACK

How stacks are accessed in the 8051...

- Pulling contents off the stack back into the CPU register is called **POP**.
- The job of the SP is very critical when the “push” and “pop” actions are performed.

NOTES:

- a) The upper limit of the stack is RAM locations 30 – 7FH.
- b) Locations 08 – 1F can be used for the stack as well.
- c) If more than 24 bytes (08 to 1FH =24 bytes) of stack is required, the instruction “MOV , SP, #xx” can be used.



8051 REGISTER BANKS AND STACK

Stack and bank 1 conflict

- Since $SP = 07$ when the 8051 is powered up, the 1st location of the stack is RAM location 08, which belongs to register R0 of register bank 1.
- In other words, register bank 1 and the stack are using the same memory location. (**Conflict!!!**)
- Solution is to re-allocate another section of RAM to the stack.
- Example: can allocate RAM locations 60H and higher to the stack.